EXHIBIT 15

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION

REDSTONE LOGICS LLC, Plaintiff, v. QUALCOMM INC. and QUALCOMM TECHNOLOGIES, INC. Defendants.	Case No. 7:24-cv-000231-ADA

PLAINTIFF'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

U.S. Patent No. 8,549,339 (the "'339 Patent[1]") teaches an innovative multi-core processor with sets of processor cores. In particular, the '339 Patent teaches various means of coordinating not just the individual cores of the multi-core processor but the sets of processor cores that operate as a unit. *See* '339 Patent at 2:61-3:15. While previous techniques focused on coordination among individual cores, the '339 Patent focuses on coordination as to sets of cores. Despite this focus, Qualcomm's claim construction arguments disregard the importance of these sets.

Throughout its opening brief, Qualcomm disregards inconvenient portions of the claims to support its position. For the first term, Qualcomm ignores what the first and second clock signals are: inputs to PLLs of ***sets*** of cores. For the second, Qualcomm asks the Court to take on faith their expert's conclusion. And for the last term, Qualcomm misconstrues the basic grammar of the claim to ask questions a POSITA would never face. Because each of Qualcomm's arguments fail, the Court should give each term its plain and ordinary meaning.

II. DISPUTED TERMS REQUIRING CONSTRUCTION

A. Term 1: "the first clock signal is independent from the second clock signal"

'339 Patent Claims	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 1, 21	**Plain and ordinary meaning**	**Plain and ordinary, meaning, where the plain and ordinary meaning requires that the first and second clock signals are provided by or processed (i.e., divided or multiplied) from different reference oscillator clocks**

[1] The '339 Patent is part of the record at Dkts. 27-2, 14-1, 13-1, and 1-1.

The Independent[2] Term is simple and clear on its face, a first signal that does not depend on a particular second signal. But Qualcomm asks the Court to consider a third signal that it contends both signals cannot both depend from together. Because consideration of such a third signal has no basis in the claim language, the intrinsic record, and Qualcomm can identify nowhere in the relevant art where "independence" of two signals implicates a third signal, Qualcomm's construction must be rejected. The Court should instead adopt the construction it found in the *NXP* action referenced by Qualcomm: "plain-and-ordinary meaning, wherein the plain meaning does not require that the first and second clock signals depend from different reference oscillator clocks." Dkt. 27-11 at 2.

This plain meaning is clear when the prosecution history around the relevant amendment is considered. During prosecution, the Examiner initial rejected the independent claims as anticipated by Jacobowitz. Dkt. No. 27-7. In an Examiner Interview, the Applicant argued that Jacobowitz did not include a first and second clock signal because it offered only a single clock signal provided to both local oscilators/PLLs disclosed by Jacobowitz, not two "different/independent clock signals" as shown in Figure 3 of the patent. *See* Dkt. No. 27-8 at 3. The Examiner agreed that Jacobowtiz and Figure 3 were different but disagreed as to Jacobowitz disclosing the first and second clock signal. *Id*. The Examiner explained because, under the broadest reasonable interpretation, the present claim language, that included no mention of any PLLs, could read not just on the signal input into Jacobowitz's local oscillators/PLLs but "also reads on the output of the PLLs shown in applicant's figure 3." *Id*. In effect, the Examiner found that the output of a single oscillator as in Jacobowitz once processed through two different local

[2] For consistency and ease of reference only, Redstone adopts Qualcomm's identification of this term as the "Independent Term."

oscillators/PLLs would be "different/independent[3]" as the Applicant suggested would distinguish Jacobowitz. With this understanding of Jacobowitz and the claims, the Applicant amended the independent claims to distinguish the input and output of the PLLs and specify that the inputs of the two PLLs must be independent:

Original Claim Language	Amended Language
1: A multi-core processor, comprising: A first set of processor cores of the multi-core processor, wherein each dynamically receive a first supply voltage and a first clock signal; A second set of processor cores of the multi-core processor, wherein each processor core form the second set of processor cores is configured to dynamically receive a second supply voltage and a second clock signal; and An interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.	1: A multi-core processor, comprising: A first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input; A second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and An interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

Dkt. No. 27-9 at 4.

The new claims did not read on Jacobowitz even under the broadest reasonable interpretation. The applicant explained Jacobowitz fails to teach "a first output clock signal of a

[3] Redstone does not argue "independent" should be construed to mean "different," rather, Redstone observes that "different" is the only clarification on the plain meaning of "independent" actually supported by the intrinsic record.

first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal as input" or "the first clock signal is independent form the second clock signal," because Jacobowitz merely distributes a single signal, V_R, to the local oscillators. *Id*. at 10-11. The first and second clock signals cannot be the same signal as one signal is not two signals and a single signal cannot be independent of itself. Because the claims now distinguished between the input and output signals of the PLLs it is irrelevant that Jacobowitz's output clock signals are independent of each other as was previously critical[4].

The only other location the Applicant or Examiner consider "independent" is with Kim[5]. This discussion aligns with the discussion of Jacobowitz and the Court's construction that "independence" is unrelated to a reference oscillator. The Applicant first explains that Kim fails to disclose the claimed voltage arrangement, including that the voltage signals are independent because "Kim ***discloses having each core, not a set of processor cores***, received a V_{DD}(i.e., V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4})." *Id*. at 10 (emphasis added). In other words, there is not first and second voltage because the claimed first and second voltage supply sets of cores, not individual cores and no voltage in Kim supplies more than a single core. Without the claimed voltages, they cannot meet any of the further limitations, such as being independent of one another.

The Applicant further explains Kim fails to disclose the claimed clock signal arrangement. The Applicant explained Kim's "apparatus comprising a multi-core processor … having a single clock source … [that] is then processed … and ***provided to each of the cores***" does not disclose any of the claimed clock signals or that the first and second clock signals are independent. *Id*. at

[4] The applicant also distinguished the voltage architecture of Jacobowitz, explaining "Jacobowitz is silent with respect to at least the recited different sets of processor cores configured to receive independent supply voltages." *See* Dkt. 27-9 at 9.

[5] Notably, despite being the central basis for Qualcomm's prosecution history argument, the Examiner never considered Kim as part of an obviousness ground for the independent claims. *See* Dkt. 27-7 at 8.

10-11 (emphasis added). The Applicant repeats this for claims 10-11, 15, 18, and 22-23: "neither Jacobowitz nor Kim discloses having ***sets of processor cores*** configured to receive multiple and independent clock signals." *Id*. at 11 (emphasis added). The Applicant repeatedly identified the same problem for each "independent" limitation: no sets of processor cores. Because there are no sets of processor cores, there are no first and second supply voltages that they are configured to dynamically receive. The same is true of the first and second output clock signals and first and second PLLs. And the same is true for the first and second clock signals as input. Without sets of cores, these signals do not exist to be independent.

In contrast, Qualcomm contends the Court should focus entirely on the Applicant's reference to "a single clock source" to the exclusion of all else. Qualcomm argues "[b]y reciting the 'independent' language and distinguishing the language ('[i]nstead') from Kim's disclosure of multiple different clock signals fed by a 'single clock source,' the applicant expressly disclaimed a construction of the Independent Term that would encompass two different signals processed from a single clock source." *Id*. at 10. Qualcomm contends it may ignore the Applicant's reference to Kim's apparatus and "provided to each of the cores," because, counterintuitively, this would "ignore the applicant's disavowal" or that it is merely "hold[ing] patentees to the actual arguments made, not the arguments that could have been made." *Id*. at 11. Such a position is counter to the law. First, as explained above, the Applicant clearly made the argument that without sets of cores, there can be none of the claimed signals, including the clock signals. Further, there is a "'heavy presumption' that claim terms carry their full ordinary and customary meaning unless the patentee unequivocally imparted a novel meaning to those terms or expressly relinquished claim scope during prosecution." *Omega Eng'g, Inc, v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed. Cir. 2003) (internal citation removed). In *Omega*, the Federal Circuit rejected a construction that excluded

the ground the applicant "repeatedly insisted that its invention differed from the prior art" on. *Id.* at 1327. Qualcomm cannot and does not overcome the heavy presumption against disclaimer by ignoring that the applicant repeated three times that without sets of processor cores there are no claimed signals, voltage signals or clock signals, to satisfy the "independent" limitations. There is no connection, much less an express one between "independent" and a single clock source.

Qualcomm's other argument, that this discussion "inform[s] the meaning of 'independent' clock signals," also fails. *See* Dkt. No. 27 at 12. This argument relies on the same misreading of the prosecution history as Qualcomm's disavowal argument. What the applicant repeats is that Kim does not disclose sets of cores and thus cannot disclose the claimed signals or any of the claimed features of those signals (i.e. first and second, or independent). *See* Dkt. No. 27-9 at 11 ("As discussed above, neither Jacobowitz nor Kim discloses having ***sets of processor cores*** configured to receive multiple and independent clock signals."); *id.* at 10-11 ("Instead, Kim discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having a single clock source (i.e., 170 in FIG. 1 or 270 in FIG. 2). The clock signal from this single clock source is then processed (i.e., divided or multiplied and provided to ***each of the cores***."); *id.* at 10 ("Kim fails to disclose or teach … a first supply voltage and a second supply voltage which is independent from the first supply voltage, respectively. Instead, Kim discloses having ***each core, not set of processor cores,*** received a V_{DD} (i.e., V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4})."") (emphasis added). Each and every time the Applicant discussed "independent," it was to explain it is not met because the core architecture is wrong and thus no arrangement of clock signals could meet the limitations.

Beyond the prosecution history, Qualcomm argues for some ill-defined mathematical approach to "independent." Dkt. 27 at 6. But this argument is meritless and unsupported. Qualcomm imagines a "single reference oscillator approach" wherein a single oscillator is

provided to two dividers that output the input frequency divided by 2 and 4 respectively or $f_1/2$ and $f_1/4$. *Id*. Qualcomm then declares "Clock signals at $f_1/2$ and $f_1/4$ ***do not*** meet the plain and ordinary meaning of 'independent' because they remain dependent on the same input." *Id*. The only support Qualcomm has for this declaration is its own expert who provides "[b]ecause the clock frequencies $f_1/2$ and $f_1/4$ that are provided to Components 1 and 2 originate from and are mathematically derived from clock frequency f_1 of the reference oscillator, clock frequencies $f_1/2$ and $f_1/4$ are not independent." Dkt. 27-1 at ¶44. But there is no explanation or support for this notion that signals derived from a common source cannot be independent from one another. Dr. Villasenor does not, and presumably cannot, show any evidence that POSITAs at the time considered a common "mathematical[] deriv[ation]" of two signals to be a dependence of one of those signals on the other. Instead, Dr. Villasenor's opinions are entirely conclusory and thus not useful. *See Phillips v. AWH corp.*, 415 F.3d 1202, 1218-19 (Fed. Cir. 2005) ("conclusory, unsupported assertions by experts as to the definition of a claim term are not useful").

Even if this "mathematical" dependence argument is considered, it fails on its own terms. Qualcomm's example is far too simple to be representative of anything a POSITA would actually consider. First, the dividers would not simply apply a set ½ or ¼ divisor to the incoming signal. Rather, as explained in the patent, each core would provide a request for a particular clock frequency requiring a dynamic divisor. *See e.g.* Dkt. 27-2 at 4:35-63. These divisors would thus be variable, dependent on not just the required frequency but the input frequency as well.

While Qualcomm does somewhat consider a variable divisor scenario, it is still unrealistically simple. Qualcomm contends "[e]ven if two or more factors may affect the frequency of the resulting clock signals, that fails to negate the fact that each of these clock signals remains dependent upon the same reference oscillator." Dkt. 27 at 7. But this assumes the divisors do not

actively negate any changes in the reference oscillator frequency. But that is precisely what must be done to provide a requested frequency if the input signal is subject to change.

The only counter example Dr. Villasenor considers is the instance where the frequency of the single reference oscillator is 0. *See* Dkt. 27-1 at ¶45. But under that consideration, there are no "independent" clock signals when those signals rely on the same power source. Indeed, in such a scenario one could disprove "independence" by shutting the device off, no power, no clock signal. But this can be dismissed out of hand, the embodiments depicted in the figures of the '339 Patent are implemented in a single device, presumably with a singular power source. *See* '339 Patent at Figs. 1-3. Neither Qualcomm nor Dr. Villasenor provide a reasonable analysis here and should be disregarded.

Because the plan language of the claim term is clear and no alternative construction was established in the prosecution history, the Independent term should be given its plain meaning. The Court should adopt its prior construction of the Independent Term: "plain-and-ordinary meaning, wherein the plain meaning does not require that the first and second clock signals depend from different reference oscillator clocks." Dkt. 27-11 at 2.

B. Term 2: "located in a periphery of the multi-core processor"

'339 Patent Claims	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 5	**Plain and ordinary meaning**	**Indefinite**

"Periphery" has a plain, geometric, meaning to one of ordinary skill. Qualcomm's attempt to create ambiguity through unsupported, conclusory expert opinion does not meet its clear and convincing evidence burden. Because Qualcomm has nothing else, its indefiniteness argument must be rejected.

The scope of "a periphery of the multi-core processor" is clear from the intrinsic evidence. First, the patent clearly describes a "multi-core processor." The first line of the patent provides an example of a "multi-core processor," which "includes two or more independent processor cores arranged in an array." '339 Patent at 1:6-7. Claim 1 describes a particular multi-core processor with a first and second set of processor cores and an interface block coupled to both sets. *See id.* at Cl. 1. The patent goes further to illustrate the multi-core processor in Figure 1. *Id.* at 1:26-27.

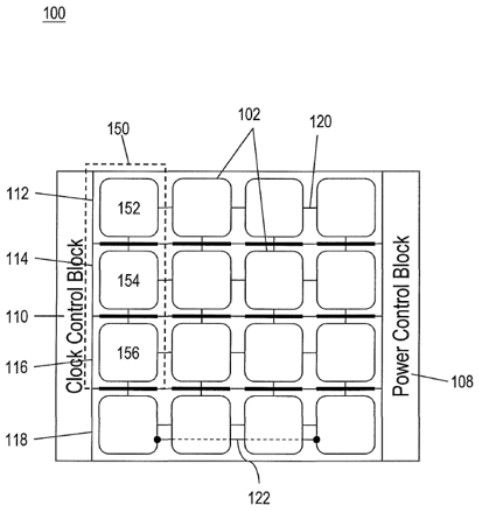
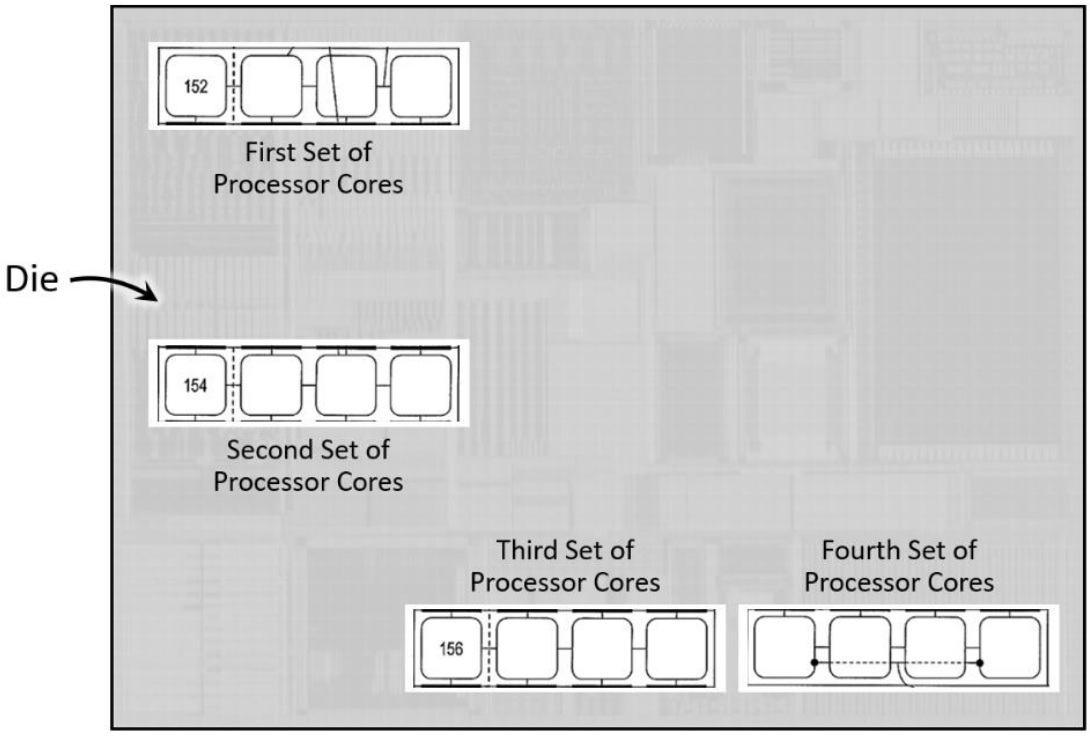


FIG. 1

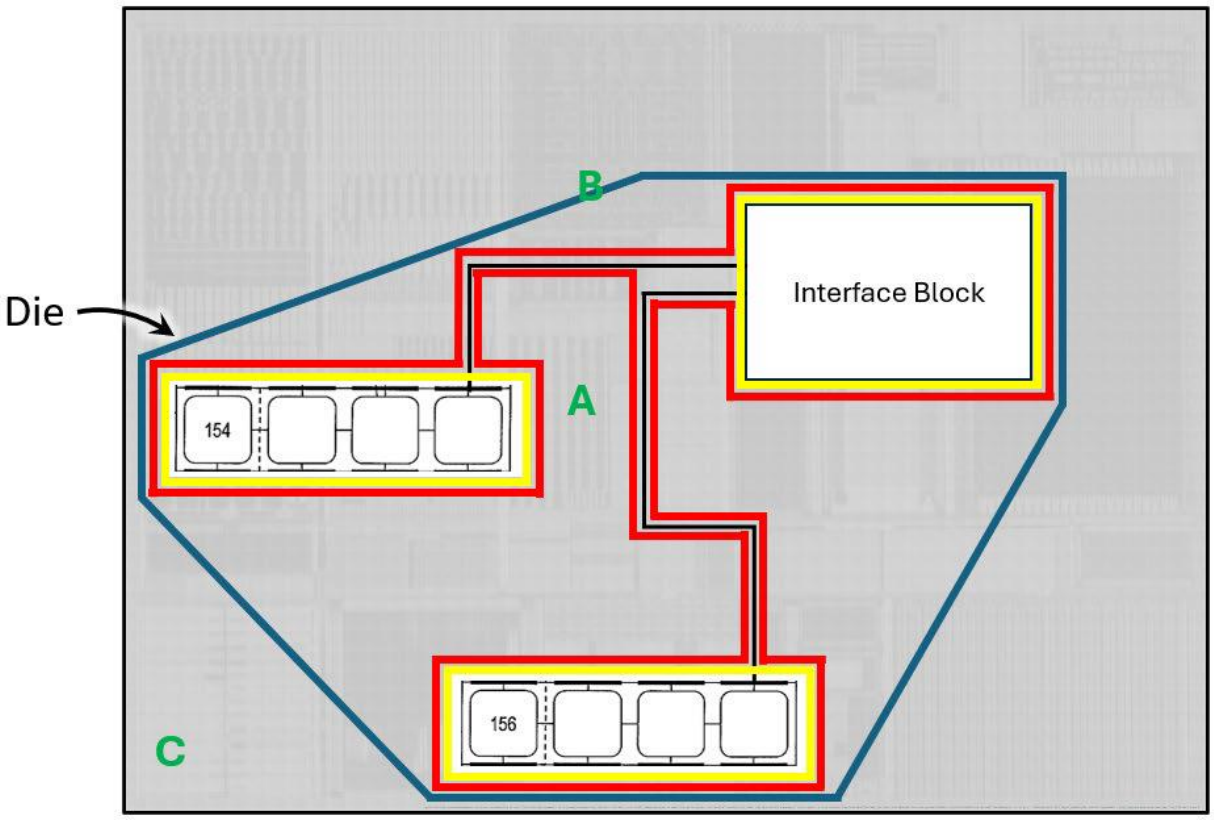
In Figure 1, the various cores are depicted as 102 with a potential set 150 of cores 152, 154, and 156 where all cores are interconnected through an interface circuit 120. *See id.* at 2:4-40; 3:16-26. The specification provides that "[i]n some implementations, the power control block 108 and the clock control block 110 may be arranged at two different sides of the multi-core processor 100 as shown in FIG. 1." '339 at 2:34-36. The specification thus clarifies the metes and bounds of the multi-core processor, placing the control blocks at its edge or periphery of the Figure 1 example. There is no ambiguity in either term and no need to consider extrinsic evidence.

But Qualcomm would ignore this clear explanation of a readily understood term for examples of distributed architectures with no support beyond conclusory expert opinions. Qualcomm's contention that "a POSITA understands that the multiple processor cores may be placed around the semiconductor die, as shown below:"



, Dkt. 27 at 14, is a half-truth. Redstone agrees many different arrangements of sets of cores may exist, but they are still bound to a rational and useful arrangement. The above example has four sets of isolated cores with no apparent power, data, or frequency inputs. Perhaps Qualcomm intended that such necessities of a working system to be implied by the noise in the background, but a POSITA would expect these requirements and would not consider a multi-core processor to exist without them. Worse, Qualcomm has no evidence a POSITA would consider this or any other particular arrangement. Instead, it cites only is own expert's declaration wherein Dr. Villasenor in turn cites nothing. Again, a conclusory expert opinion is useless. *See Phillips*, 415 F.3d at 1218-19.

Qualcomm does provide a moderately more detailed but no more supported example:



. Dkt. 27 at 15. Qualcomm's second example includes one more claimed component, the interface block, but such an example is still deficient. First, there is no support for the notion that such an arrangeemnt would exist or would be considered by a POSITA when contemplating the scope of "periphery." Again, Qualcomm cites its own expert's conclusory declaration. Dkt. 27 at 15. The only support Dr. Villasenor gives for this arrangement ever being considered by a POSITA is that "the depicted component placement would not be unsuusal due to the need to use some of the real estate on the chip for functionalities other than processor cores." Dkt. 27-1 at ¶71. There is no citation to any such "not [] unusual" arrangement ever exisiting or explanation for how "real estate" needs would result in such a sparatic arrangement of connections. *Id*. Without support, Qualcomm's example should be disregarded. *See Phillips*, 415 F.3d at 1218-19.

In particular, "[a]ny fact critical to a holding on indefiniteness … must be proven by the challenger by clear and convincing evidence." *Intel Corp. v. VIA Techs., Inc.*, 319 F.3d 1357, 1366 (Fed. Cir. 2003). Without these example architectures, Qualcomm has no argument. Dkt. 27 at 13-16 (making no argument that "periphery" or "multi-core processor" are inherently indefinite). Thus, because these examples are not supported by any evidence, much less clear and convincing evidence, Qualcomm cannot meet its burden to show this term is indefinite.

The few cases cited by Qualcomm do not hold otherwise. Rather, in the example case Qualcomm recites, the ambiguity of the term was implicit on its face. *Interval Licensing LLC v. AOL, Inc.* addressed the meaning of "unobtrusive manner," a term implicitly reliant "on the unpredictable vagaries of any one person's opinion." 766 F.3d 1364, 1373–74 (Fed. Cir. 2014). Qualcomm does not and cannot contend the same here.

A POSITA readily understands the scope of "located in a periphery of the multi-core processor." Even if this is not apparent from the patent, Qualcomm has not met its burden of showing by clear and convincing evidence that a POSITA would have any trouble with the scope of the term. The disputed term should be given its plain and ordinary meaning.

C. Term 3: "located in a common region that is substantially central to the first set of cores and second set of processor cores"

'339 Patent Claims	Redstone's Proposed Construction	Defendant's Proposed Construction
Claims 14	**Plain and ordinary meaning**	**Indefinite**

Qualcomm argues both "common region" and "substantially central" render this term indefinite. But Qualcomm misapplies the law as to both. For the first, Qualcomm misapplies the

doctrine of claim differentiation. For the second, Qualcomm ignores the teachings of the specification. As such, this term should be given its plain and ordinary meaning.

"Region" and "common region" are clearly described in the patent. Rather than merely relating to an undefined area, "region" is used throughout the patent to refer to sections of the multi-core processor. *See* '339 Patent at 2:20-21 ("The multi-core processor 100 may be further divided into regions.") The specification explains these regions may "correspond to rows of the two-dimensional array, and the regions may or may not be overlapping." *Id*. at 2:22-23. These "two-dimensional array[s]" are the rows of processors or stripes that can make up sets of processor cores. *Id*. at 2:24-27. This use is continued throughout the claims. *See e.g. id*. at Cl. 8 ("wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.") A POSITA would understand that a "region" corresponds with the subdivision of the multi-core processor containing the claimed sets of processor cores.

Understanding "region" is a subdivision of the multi-core processor containing the claimed sets of processor cores, "common region" is no mystery. In claim 14 it refers to the region common to the claimed first and second sets of processor cores and contains the control blocks. *See* Cl. 14. Qualcomm agrees, recognizing "common region" refers to a part of the multi-core processor shared by the first and second sets of processor cores, though attempts to discredit this understanding through claim differentiation. *See* Dkt. 27 at 20 ("one possible interpretation of a common region shared by first and second sets of processor cores could be that the sets of processor cores 'overlap' in physical space").

While Qualcomm attempts to dispute this plain meaning of "common region" through claim differentiation, the claim differentiation doctrine cannot be used to support a finding of

indefiniteness. Claim differentiation creates a *rebuttable* presumption of non-redundant claims. *See Comark Communications, Inc. v. Harris Corp*., 156 F.3d 1182, 1187, 48 U.S.P.Q.2d 1001 (Fed. Cir. 1998) ("While we recognize that the doctrine of claim differentiation is not a hard and fast rule of construction, it does create a presumption that each claim in a patent has a different scope."). The Federal Circuit has explained that this cannon is not an absolute, "where neither the plain meaning nor the patent itself commands a difference in scope between two terms, they may be construed identically." *Power Mosfet Technologies, L.L.C. v. Siemens AG*, 378 F.3d 1396, 1409–10, 72 U.S.P.Q.2d 1129 (Fed. Cir. 2004). Here, if, as Defendant argues, claim 14 has an overlapping meaning with claim 9, that meaning is mandated by the plain meaning and the patent itself and thus the claims should be construed identically, not indefinitely. Even if claim differentiation could result in indefiniteness, claim differentiation is inapplicable. There are a variety of other differences between claim 14 and claim 9. For instance, claim 9 does not recite "one or more control blocks." Claim 14 does. Further, claim 9 recites two regions, claim 14 recites only one. With many differences between claim 9 and 14, there is no risk that the Court finding claim 14 definite would render any claim superfluous. Considering even Qualcomm recognizes the scope of "common region," "common region" cannot be the basis for finding claim 14 indefinite.

Qualcomm's argument as to "substantially central" fares no better. For a "substantially" term to be definite, "[a]ll that is required is some standard for measuring the term of degree." *Exmark Mfg. Co. Inc. v. Briggs & Stratton Power Prods. Grp., LLC*, 879 F.3d 1332, 1346 (Fed. Cir. 2018). The patent provides that guidance.

First, Qualcomm misconstrues the grammar of claim 14 to suggest the control blocks are "substantially central." This is not quite true. Rather, claim 14 provides that it is the "common

region that is substantially central" and the "control blocks [are] located in [the] common region." As explained above, "common region" is the region of the multi-core processor that is common to the first and second set of processor cores. Further requiring that this region to contain the control blocks and be "substantially central" to the sets of processor cores is rudimentary and described in the specification.

The patent describes three possibilities for the location of the control blocks: "two different sides of the multicore processor," "the same side of the multi-core processor," or "in a common area located near the center of the multi-core processor." '339 Patent at 2:31-40. Put differently, the patent describes putting the control blocks on the sides of the processor or within the processor. A POSITA would understand claim 14 is directed to this latter example where a common area/region is central and contains the control blocks. As such a POSITA would understand that for the "common region" of two sets of cores to be substantially central merely requires it to be within the multi-core processor. While "within the multi-core processor" is a broad construction, breadth is not indefiniteness. *BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1367 (Fed. Cir. 2017) ("the inference of indefiniteness simply from the scope finding is legally incorrect: 'breadth is not indefiniteness.'"). This meets the Federal Circuit's requirement for "some standard for measuring the term of degree."

To the extent Qualcomm argues this reading of "common region" as simple a subdivision of the multi-core processor shared by the two sets of processors and "substantially central" as merely within the multi-core processor renders one or the other a superfluity, such superfluity is irrelevant. Even if a subdivision of the multi-core processor within the multi-core processor is redundant, that does not and cannot render the claim indefinite. As explained above, the cannon against superfluity is not absolute, "where neither the plain meaning nor the patent itself commands

a difference in scope between two terms, they may be construed identically." *Power Mosfet,* 378 F.3d at 1409–10.

In contrast, Qualcomm asks the wrong question. "[W]hether the control blocks are 'substantially central' by virtue of being equidistant from each set of cores" or otherwise, *see* Dkt. 27 at 18, misconstrues the claim. Again, it is the "common region" that is "substantially central" not the control blocks contained within the "common region." *See* '339 Patent at Cl. 14. As far as claim 14 is concerned the control blocks can be anywhere within the "common region." Considering Qualcomm's figures, the question is whether a "common region" exists in the Figure H and I examples within the multi-core processor and if the control blocks are within that region. Given the anemic disclosure of these examples, showing only sets of cores with no connections or interface blocks, it cannot be determined.

Even if these figures were directed to the correct question, they should still be disregarded. Just as with term 2, Dr. Villasenor has created these example arrangements without regard to what a POSITA might actually consider. *See* Dkt. No. 27-1 at ¶¶85-86. Unlike the examples he prepared for term 2, here there is no suggestion a POSITA would ever consider such an arrangement. Such conclusory opinions cannot meet Qualcomm's clear and convincing burden. *See Intel Corp.*, 319 F.3d at 1366.

For these reasons, Qualcomm has not shown by clear and convincing evidence that Claim 14 is indefinite. Claim 14 should be given its plain and ordinary meaning.

III. CONCLUSION

For the reasons provided above, all disputed terms should be given their plain and ordinary meaning. Defendant has failed to meet its burden to show any term is indefinite.

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CERTIFICATE OF SERVICE

I certify that on April 25, 2025, a true and correct copy of the foregoing document was electronically filed with the Court and served on all parties of record via the Court's CM/ECF system.

/s/ Reza Mirzaie
Reza Mirzaie